REMARKS

Claims 18-27 are pending in this application. By this Amendment, claims 18 and 21 have been amended. Claim 18 is independent. Reconsideration of the application is respectfully requested.

I. Amendment

The amendment to claim 21 corrects antecedent basis issues and the amendment to claim 18 improves clarity. No new matter is added.

II. Rejection Under 35 U.S.C. §112, Second Paragraph

The Office Action rejects claims 21-24 under 35 U.S.C. §112, second paragraph. Claim 21 has been amended in accordance with the Examiner's suggestion. Withdrawal of the rejection is respectfully requested.

III. The Claims Define Patentable Subject Matter

The Office Action rejects claims 18-22 and 25-27 under 35 U.S.C. §103(a) over U.S. Patent No. 3,737,858 to Turner et al. (Turner) in view of U.S. Patent No. 6,175,889 to Olarig; and rejects claims 23 and 24 under 35 U.S.C. §103(a) over Turner in view of Olarig and further in view of U.S. Patent Application Publication No. 2002/0063661 to Comiskey et al. (Comiskey). These rejections are respectfully traversed.

Independent claim 18 recites, *inter alia*, "an initialization phase, where the control circuit successively addresses the microsystems by their respective identification codes and stores a reduced addressing code in the respective registers of the microsystems." The applied references fail to teach or suggest the recited features of independent claim 18.

The Office Action acknowledges that Turner does not disclose an initialization phase that stores a reduced addressing code in the respective registers of the microsystems. However, the Office Action alleges that Olarig discloses such an initialization phase.

Turner uses only one kind of code (a number assigned to a transducer, corresponding to an addressing code) and does not use two different codes (identification code and addressing code), one of them being a reduced code. Thus, Turner does not disclose an identification code and a reduced addressing code. Turner also fails to disclose that each microsystem comprises an identification code and a reduced addressing code.

Olarig discloses a computer system motherboard comprising different physical PCI-X buses, for example Buses A, B and C. See Fig. 4 of Olarig. A plurality of PCI-X devices can be connected on each bus such as devices 1 to 16. See col. 17, lines 22 and 23. A range of memory addresses is associated with each PCI-X device. Each PCI-X device comprises a top address range register and a bottom address range register. See col. 10, line 59 to col. 11, line 8. The values of these registers are set by software during the startup of the computer ("a computer system POST") or dynamically afterwards. See col. 11, lines 2-4. Address ranges of each PCI-X device are stored in configuration registers during startup. See col. 11, lines 47-54. Thus, when a controller wants to communicate with a particular memory address, the controller is able to check the configuration registers in order to determine the physical PCI-X bus (A, B, C) on which the PCI-X device (1 to 16), having an address range comprising this particular address, is connected. See col. 17, lines 22 and 23. Then, a transaction can be sent to the appropriate bus. All the PCI-X devices connected to the bus are going to receive the transaction and the device having an address range containing the particular address will use this transaction. This can avoid concurrent transactions issues from appearing.

The initialization phase of Olarig enables the storage of an address range to each PCI-X devices with each PCI-X device being identified by a unique device number. See col. 17, lines 22 and 23 of Olarig. Each address range is defined by top and bottom address values and is equivalent to a plurality of different addresses associated with different PCI-X devices. However, such an address range does not disclose a reduced PCI-X address. The

initialization phase of Olarig does not correspond to the storage of a reduced addressing code to each PCI-X device. Also, this address range is then stored in a register of a controller in order to permit to a transaction to be routed to a unique PCI-X bus and not in a register of the PCI-X device. Thus, Olarig fails to disclose an initialization phase that stores a reduced addressing code in the respective registers of the Microsystems, as recited in claim 18. Comiskey fails to cure the deficiencies of Turner and Olarig. Accordingly, the applied references, alone or in combination, fail to teach or suggest the recited features of independent claim 18.

The dependent claims are allowable at least due to their dependence on allowable independent claim 18 and for the additional features they recite.

Accordingly, withdrawal of the rejections of the claims is respectfully requested.

IV. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the application are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

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